Before You Begin

INTRODUCTION

It is important to be aware of the system considerations listed below before installing your BXT7059 or BXTS7059 (7059-xxx) SHB. System performance may be affected by incorrect usage of these features.

DDR3 MEMORY

Trenton recommends ECC registered DDR3-1600 Mini-DIMM memory modules for use on the BXT7059 / BXTS7059 SHBs and these ECC registered (72-bit) DDR3 Mini-DIMMs must be PC3-12800 compliant. Unbuffered ECC DDR3 Mini-DIMMs are also supported on the BXT/BXTS boards, however you cannot mix the ECC registered and unbuffered ECC memory types on the same board.

Each processor on a BXT7059 / BXTS7059 SHB supports three direct-connect DDR3 memory interfaces. The maximum possible memory interface speed obtained depends on the specific Intel® Xeon® E5-2400 v2 or Intel® Xeon® E5-2400 series processor(s) used on the board and other board configuration options listed in the notes section below. The table below illustrates the maximum DDR3 **memory speed** supported as a function of each specific Intel® Xeon® processor when using the recommended PC3-12800 compliant Mini-DIMM modules and an SHB with the latest BIOS support.

Max. DDR3 Speed	Processor	Cores / Threads	Cache	Long-Life Availability	Maximum Thermal Design Power (TDP)	Operating Temperature Range*
DDR3-1600	Intel® Xeon® E5-2450 v2	8 / 16	20MB	Yes	95W	0°C to 40°C
DDR3-1600	Intel® Xeon® E5-2430 v2	6 / 12	15MB	Yes	80W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L v2	10 / 20	25MB	Yes	70W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2428L v2	8 / 16	20MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L v2	6 / 12	15MB	Yes	50W	0°C to 50°C
DDR3-1600	Intel® Xeon® E5-2448L	8 / 16	20MB	Yes	70W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2430	6 / 12	15MB	Yes	95W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2428L	6 / 12	15MB	Yes	60W	0°C to 50°C
DDR3-1333	Intel® Xeon® E5-2418L	4 / 8	10MB	Yes	50W	0°C to 50°C

*Requires a continuous airflow across the board of 350LFM.

NOTES:

- To maximize system performance and reliability, Trenton recommends populating each memory channel with DDR3-1600 Mini-DIMMs and using an even number of memory modules.
- All memory modules must have gold contacts.
- Low voltage (DDR3L) Mini-DIMMs are not supported.
- The SHB supports the following memory module memory latency timings:
  - 9-9-9 for 1600MHz DDR3 Mini-DIMMs
- Populate the memory sockets starting with the Mini-DIMM socket closest to the CPU and work your way toward the edges of the SHB as illustrated in the chart below:

Mini-DIMM Population Order	CPU0*	Mini-DIMM Population Order	CPU1*
1	BK00	1a	BK10
2	BK01	2a	BK11
3	BK02	3a	BK12

- *CPU0 and CPU1 are both available on BXT7059 SHBs.
- Using a balanced memory population approach with the BXT7059 configuration; meaning an equal number of Mini-DIMMs per processor, ensures maximum memory interface performance.

The memory DIMMs on the SHB connect directly to the CPU and at least one memory module must be installed on the board. The BXTS7059 SHB versions feature one processor; however, memory slots BK10, BK11 and BK12 are installed on the SHB but are not active in this single-processor board version.

SAS / SATA RAID Operation

The SHB's Intel® C604 Platform Controller Hub (PCH) features Intel® Rapid Storage Technology, which enables SHB support for RAID 0, 1 and 10 implementations. To configure the SAS / SATA ports as RAID drives, you must install the Intel® RST enterprise driver software. This link takes you to version 3.2 that was tested and validated on the SHB. A later version 3.5 is also available for download, but this version has not been tested on the board. Links to both driver versions are located on Trenton's website by accessing the Downloads tab of either the BXT7059 or the BXTS7059 product detail web pages or the RAID Drivers section of the Technical Support page.

Mouse/Keyboard "Y" Cable

If you have an IOB33 I/O board in your system and you are using a "Y" cable attached to the bracket mounted mouse/keyboard mini Din connector, be sure to use Trenton's "Y" cable, part number 5886-000. Using a non-Trenton cable may result in improper SHB operation**.**

PCI Express 3.0 Links and PICMG® 1.3 Backplanes

The A0 through A3 PCI Express® links on the SHB connect directly to processor CPU0. These links can operate as either PCI Express 3.0, 2.0 or 1.1 links based on the end-point devices on the backplane that are connected to the SHB and the backplane's PCIe link design itself. In addition to automatically configuring themselves for either PCIe 3.0, 2.0 or 1.1 operations, the links also configure themselves for either graphics or server-class operations. In other words, the multiple x4 links from CPU0 (links A0, A1, A2 and A3) can be utilized on a backplane as a single x16 PCIe electrical link, two x8 links, or four x4 links. CPU0's x4 links can train down to x1 links, but cannot bifurcate into multiple x1 links. PCIe link B0 comes from the board's PCH and is a PCIe 2.0 interface. Link B0 has a x4 default configuration that can automatically bifurcate into four, x1 PCIe links. An optional PEX10 module connects to the second processor (CPU1) on the dual-processor BXT7059 board to extend the PICMG 1.3 base specification by providing four additional x4 PCIe links. These additional links may also operate as either PCI Express 3.0, 2.0 or 1.1 links and can be combined into one x16, or two x8 or four x4 PCIe interfaces on a PEX10-supported PICMG 1.3 backplane. This BXT7059 capability provides additional PCI Express bandwidth and option card support in the system design. Refer to the *PCI Express® Reference* chapter and to *Appendix C - PCI Express Backplane Usage* of the BXT7059 / BXTS7059 Hardware Manual for more information.

A Word About PCI Express 3.0 Interfaces

PCIe 3.0 doubles the PCIe 2.0 per lane interface speed from 500MB/s (5GT/s) to 1GB/s (8 GT/s) via speed changes and protocol enhancements. As with all previous versions of the PCI Express specification, the PCIe 3.0 interface is backwards compatible and will run Gen 3, Gen 2 and Gen 1.1 I/O cards on the same interface link. Running a PCIe 3.0 target device such as a Gen 3 I/O card at the actual PCIe 3.0 interface speed of 1GB/s **requires** that the PCIe 3.0 link from the root complex (i.e. the processor on the BXT7059) to the target card be tuned and optimized to meet the speed requirements of PCI Express 3.0. If these tuning conditions are slightly off and not fully optimized, then the interface will operate at a slower interface speed. Contact Trenton for more details regarding the specifics of your particular PCIe 3.0 implementation.

PICMG 1.3 Backplane I/O

The BXT7059 / BXTS7059 enable the following PICMG 1.3 backplane I/O connectivity via the SHB's edge connector C:

- Four USB 2.0 interfaces
- One 10/100Base-T Ethernet interface
- One SATA/300 interface

Off-Board Video Card Usage

If the system design requires an off-board video card, then the card must be placed in a backplane slot driven with PCI Express links from the BXT7059's first processor. This is an Aptio® 4.x BIOS limitation that may be corrected in future software revisions. Listed below are the acceptable BPC7041 backplane slots for use with an off-board video card:

BPC7041 - Card slot PCIe6, PCIe7, PCIe8, PCIe9 or PCIe10

BIOS

The BXT7059 and BXTS7059 feature the Aptio® 4.x BIOS from American Megatrends, Inc. (AMI) with a ROM-resident setup utility called the Aptio Text Setup Environment or TSE. Details of the Aptio TSE are provided in the separate *BXT7059 / BXTS7059 BIOS Technical Reference* manual.

Operating Systems

Trenton's BXT7059 and BXTS7059 have been tested using a number of popular and readily available operating systems including: Microsoft Windows XP X64, Windows Server 2003, Windows Server 2008 R2, Windows 7 and a number of variations of Linux including Red Hat. This testing process confirms the SHB's PCI Express interface and device I/O functionality. Trenton does not recommend using the Microsoft Windows XP32 SP2 or SP3 operating system due to limited functionality concerns. Contact Trenton Tech Support for additional information.

HDD STATUS LED OPERATION (P12)

The operation of any HDD status LED connected to P12 will vary based on the system's OS install and the board's BIOS settings. If SAS OPRom is enabled [i.e. this is the board's BIOS default setting, see the South Bridge Configuration section in the *BXT7059 / BXTS7059 BIOS Manual* and the driver that supports the SAS controller is installed in the OS, then the HDD LED will function as expected. Expected mode of operation is that the HDD LED comes on solid during POST and as soon as the OS starts to boot, the LED will start flashing indicating HDD activity and will go off when there is no HDD activity. If the SAS OPRom setting is enabled in the board's BIOS, but no SAS driver is installed in the OS then the system's HDD LED will turn on solid and not go out until the SAS driver is installed. This condition exists regardless if a SAS drive is connected or not connected to one of the SAS ports (P31, P32, P35 or P36) on the SHB.

FOR MORE INFORMATION

For more information on any of these features, refer to the appropriate sections *BXT7059 / BXTS7059 Hardware Technical Reference Manual*. The BIOS and hardware technical reference manuals are available under the **Downloads** tab on the BXT7059 or BXTS7059 web pages.